[a counter that is connected to control said instruction supplying means in order to supply the instructions in succession;]

instruction decoding means [that are connected to receive the instructions in succession from the instruction supplying means] for configuring said instruction supplying means to select from said instruction register an operand associated with one of said instructions from said first of said instruction groups[; and

said counter being connected to said instruction decoding means to receive counter control signals from said instruction decoding means].

72(Amended). The microprocessor system of claim 71 [further comprising:] wherein said instruction decoding means further includes means, responsive to a SKIP instruction in said instruction register, for configuring said instruction supplying means to skip one or more of said one or more sequential instructions during transfer thereof to said central processing unit [that are configured to supply a reset using said counter control signals to said counter and to supply control signals to said instruction fetching means such that the next said fixed-length instruction group is supplied to said instruction register in response to a SKIP instruction in said multiple sequential instructions].

73(Amended). The microprocessor system of claim 72 further comprising:

means for [to produce a "TRUE" or "FALSE" outcome from] determining whether [the testing of] a predefined condition exists within said microprocessor system, and [said]

means for controlling response of said instruction supplying means to said SKIP instruction based on existence of said predefined condition [response to a SKIP instruction modified to occur when said outcome is "TRUE."]

74(Amended). The microprocessor system of claim 71 further comprising:

a loop counter that is connected to receive a decrement control signal from said instruction decoding means[;], said instruction decoding means [that are] being configured to supply [a reset using said counter control signals to said counter and] said [a] decrement

control signal to said loop counter in response to a MICROLOOP instruction within one of said one or more sequential instructions received from said instruction supplying means [in said multiple sequential instructions].

75(Amended). The microprocessor system of claim 74 further comprising:

means for [to produce a "TRUE" or "FALSE" outcome from] determining whether [the testing of] a predefined condition exists within said microprocessor system, and [said]

means for controlling response of said instruction decoding means to [a] said MICROLOOP instruction [modified to occur when said outcome is "TRUE"] based on existence of said predefined condition.

77(Amended). The microprocessor system of claim 71 wherein said [further comprising] instruction decoding means [that are configured to supply a reset using said counter control signals to said counter and to supply] includes means for supplying control signals to said instruction fetching means such that a subsequent [fixed-length] one of said instruction [group] groups is supplied to said instruction register, and for configuring said instruction supplying means to supply to said central processing unit [the] a remainder of [said] a current one of said [fixed-length] instruction [group] groups as [an] another operand[in response to a variable-length-operand-using instruction in said multiple sequential instructions].

78(Amended). The microprocessor system of claim 71 [further comprising] wherein said instruction decoding means [that are configured] configures said instruction supplying means to supply to said central processing unit a last byte of [said fixed-length] a current of said instruction [group] groups as [an] another operand in response to [a last-byte-operand-using] one of [instruction in] said [multiple] one or more sequential instructions within said current one of said instruction groups.

79(Amended). The microprocessor system of claim 71 [further comprising] wherein said instruction decoding means [that] are configured to supply control signals to said

instruction fetching means such that a subsequent one of said [fixed-length] instruction [group] groups is supplied as an operand in response to [a extra-group-operand-using] one of [instruction in] said [multiple] one or more sequential instructions within said first of said instruction groups.

80(Amended) The microprocessor system of claim 71 [further comprising] wherein said instruction decoding means [that] are configured to supply control signals to said instruction fetching means such that a subsequent one of [the next] said [fixed-length] instruction [group] groups supplied to said instruction register is determined in response to a branch-type instruction in said [multiple] one or more sequential instructions within said first of said instruction groups.

81(Amended). The microprocessor system of claim 77 [or 80, wherein said branch-type instruction is a variable-length-operand-using instruction] wherein said instruction decoding means are configured to supply control signals to said instruction fetching means such that a subsequent one of said instruction groups supplied to said instruction register is determined in response to a branch-type instruction in said one or more sequential instructions within said first of said instruction groups.

82(Amended). The microprocessor system of claim 80 further comprising a counter connected to said instruction supplying means, said counter providing a count signal indicative of an instruction of said subsequent one of said instruction groups that is to be provided to said central processing unit by said instruction supplying means, said counter being [the supplying of a reset using said counter control signals to said counter] reset in response to [a] receipt by said instruction decoding means of said branch-type instruction in said one or more sequential instructions.

83(Amended). The microprocessor system of claim 80 further comprising [a] means for [to produce a "TRUE" or "FALSE" outcome from] determining whether [the testing of] a predefined condition exists within said microprocessor system, and [said]

means for controlling response of said instruction decoding means to [a] said branch-type instruction [modified to occur when said outcome is "TRUE"] based on existence of said predefined condition.

84(Amended). The microprocessor system of claim 71 wherein said instruction fetching means fetches said [multiple] one or more sequential instructions in parallel for each of said [fixed-length] instruction groups [group] in a single memory cycle.

85(Amended). The microprocessor system of claim 71 further comprising:

memory access testing means for testing [the] said first [current] of said instruction groups [group] to determine if [the multiple] said one or more sequential instructions require a memory access; and

if said memory access testing means determine a memory access is not required, then supplying of control signals to said instruction fetching means to fetch the next instruction group during the execution of [the current] said first of said instruction groups [group].

Please add the following new claims 86-100:

86. The microprocessor system of claim 80 further comprising a counter connected to said instruction supplying means, said instruction supplying means including means for gating said sequential instructions within said instruction register to said central processing unit based on signals produced by said counter.

87. The microprocessor of claim 71 wherein said instruction supplying means includes:

a counter connected to said instruction decoding means,

a decoder connected to an output of said counter, and

a plurality of gates interposed between said instruction register and said central processing unit, said gates being controlled by signals from said decoder.

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88. The microprocessor of claim 71 wherein said instruction decoding means includes means for determining a width of said operand, said width being related to position in said instruction register of said one of said instructions of said first of said instruction groups.

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89. The microprocessor of claim 71 wherein said first of said instruction groups includes a first instruction and multiple operand bytes, said instruction decoding means including means for determining a width of said operand associated with said first instruction based on position of said first instruction within said instruction register.

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90. The microprocessor of claim 89 wherein said instruction supplying means includes gating means for selecting one or more of said multiple operand bytes within said instruction register corresponding to said operand.

91. A microprocessor system comprising:

a central processing unit;

an instruction register operatively coupled to said central processing unit;

instruction fetching means for providing instruction groups to said instruction register wherein certain of said instruction groups include one or more sequential instructions;

instruction supplying means for successively coupling said one or more sequential instructions of said certain of said instruction groups to said central processing unit; and

instruction decoding means for configuring said instruction supplying means to select operands from said instruction register associated with particular ones of said sequential instructions.

92. The microprocessor system of claim 91 wherein said instruction decoding means, upon receiving a SKIP one of said one or more sequential instructions from a current one of said instruction groups, configures said instruction fetching means to fetch a next one of said instruction groups from a memory of said microprocessor system.

93. The microprocessor system of claim 92 further including means for determining whether a predefined condition exists within said microprocessor system, and

means for controlling response of said instruction supplying means to said SKIP instruction based on existence of said predefined condition.

94. The microprocessor of claim 91 wherein said instruction supplying means includes a loop counter, said instruction decoding means providing a decrement signal to said loop counter in response to a MICROLOOP instruction within said instruction register.

95. The microprocessor system of claim 94 further comprising:

means for determining whether a predefined condition exists within said microprocessor system, and

means for controlling response of said instruction decoding means to said MICROLOOP instruction based on existence of said predefined condition.

96. The microprocessor system of claim 91 wherein said instruction decoding means includes means, responsive to ones of said sequential instructions of predetermined type, for supplying control signals to said instruction fetching means such that a subsequent one of said instruction groups is provided to said instruction register.

97. In a microprocessor system including a central processing unit, memory, and an instruction register, a method for providing instructions from said instruction register to said central processing unit comprising the steps of:

providing instruction groups to said instruction register from said memory wherein certain of said instruction groups include one or more sequential instructions;

supplying, in succession from said instruction register, said one or more sequential instructions of said certain of said instruction groups to said central processing unit; and

selecting, in accordance with position in said instruction register of one of said instructions of one of said instruction groups, an operand from said one of said instruction groups for use by said central processing unit.

98. The microprocessor of claim 96 wherein said instruction decoding means includes means for configuring said instruction supplying means to supply a remainder of a current one of said instruction groups within said instruction register as one of said operands to said central processing unit.

99. The microprocessor system of claim 91 wherein said instruction decoding means are configured to supply control signals to said instruction fetching means such that a subsequent one of said instruction groups is supplied as an operand in response to one of said one or more sequential instructions.

100. The microprocessor system of claim 96 further comprising means for determining whether a predefined condition exists within said microprocessor system, and means for controlling response of said instruction decoding means to branch-type ones of said instructions based on existence of said predefined condition.